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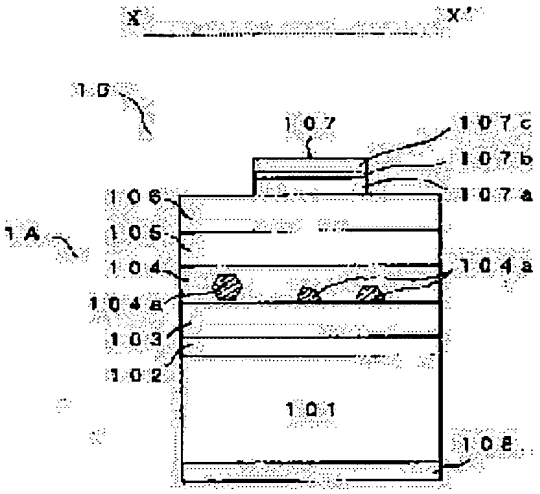
(71)Applicant : SHOWA DENKO KK
(72)Inventor : UDAGAWA TAKASHI

(54) BORON PHOSPHIDE BASED SEMICONDUCTOR ELEMENT, ITS MANUFACTURING METHOD AND LIGHT EMITTING DIODE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a technical means for obtaining an active layer having uniform indium composition when an active layer composed of group III nitride semiconductor crystal containing indium which is expressed by a general formula AlQGaRInYN (where $0 \leq Q < 1$, $0 \leq R < 1$, $0 < Y \leq 1$ and $Q+R+Y=1$) is formed on a boron phosphide based semiconductor crystal layer.
SOLUTION: An intermediate layer composed of III-V compound semiconductor is formed between a boron phosphide based semiconductor crystal layer and the active layer. The semiconductor has indium composition which is at most 1/2 of indium composition of the group III nitride semiconductor crystal layer forming the active layer. The intermediate layer is constituted from a polycrystal layer containing crystals different in a crystallinity.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The substrate which consists of a silicon (Si) single crystal, and the Lynn-ized boron system semiconducting crystal layer prepared on this substrate, With the interlayer who consists of a group-III-V-semiconducter crystal prepared on this Lynn-ized boron system semiconducting crystal layer The general formula AlQGaRInYN which sets to Y (0< Y<=1) the indium presentation established on this middle class In the Lynn-ized boron system semiconductor device equipped with the barrier layer which consists of an III group nitride semiconducting crystal expressed with (0<=Q<1, 0<=R<1, Q+R+Y=1) [however,] The Lynn-ized boron system semiconductor device characterized by being 1/2 or less [of an indium presentation (Y) of the III group nitride semiconducting crystal with which said middle class consists of a group-III-V-semiconducter crystal containing an indium, and this middle class's indium presentation makes said barrier layer].
[Claim 2] The Lynn-ized boron system semiconductor device according to claim 1 characterized by consisting of polycrystal layers which said interlayer turns into from the group-III-V-semiconducter crystal of the wurtzite mold (Wurtzite) containing the crystalline of a sphalerite mold (zinc blende).
[Claim 3] The Lynn-ized boron system semiconductor device according to claim 1 characterized by consisting of polycrystal layers which said interlayer turns into from the group-III-V-semiconducter crystal of the sphalerite mold containing the crystalline of a wurtzite mold.
[Claim 4] Said Lynn-ized boron system semiconducting crystal layer consists of Lynn-ized boron nitride and indium (BAlnDN1-deltaPdelta:0<A<=1, 0<=D<1, A+D=1, 0< delta<=1) mixed crystal. said middle class -- an alumimium nitride gallium indium (aluminumgammaGabetaInalphaN: -- 0< alpha<=0.5, 0<=beta<1, and 0<=gamma<1 --) Alpha+beta+gamma = Consist of 1 mixed crystal and said barrier layer consists of alumimium nitride gallium indium (AlQGaRInYN:0<Y<=1, 0<=Q<1, 0<=R<1, Q+R+Y=1) mixed crystal. The Lynn-ized boron system semiconductor device according to claim 1 to 3 characterized by being alpha<=0.5xY.
[Claim 5] Said Lynn-ized boron system semiconducting crystal layer consists of Lynn-ized boron and indium (BAlnDP:0<A<=1, 0<=D<1, A+D=1) mixed crystal. Said middle class consists of gallium nitride indium (GabetaInalphaN:0<alpha<=0.5, 0<=beta<1, alpha+beta = 1) mixed crystal. The Lynn-ized boron system semiconductor device according to claim 4 which a barrier layer consists of gallium nitride indium (GaRInYN:0<Y<=1, 0<=R<1, R+Y=1) mixed crystal, and is characterized by being alpha<=0.5xY.
[Claim 6] The manufacture approach of claim 1 which forms said interlayer by organic metal modified chemical vapor deposition (MOCVD law) thru/or the Lynn-ized boron system semiconductor device given in 5.
[Claim 7] The manufacture approach of the Lynn-ized boron system semiconductor device according to claim 6 which makes said interlayer's growth temperature 700 degrees C - 950 degrees C.
[Claim 8] Light emitting diode set to claim 1 thru/or 5 from the Lynn-ized boron system semiconductor device of a publication.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the technique for constituting the barrier layer excellent in the homogeneity of the presentation which brings about improvement in a component property especially with respect to the technique for constituting the Lynn-ized boron system semiconductor device which comes to have a barrier layer on the Lynn-ized boron system semiconducting crystal layer.
[0002]
[Description of the Prior Art] Conventionally, Lynn-ized boron (BP) is known as a kind of group III-V semiconducter (the Teramoto ****, "semiconductor device introduction" (refer to March 30, 1995, Baifukan Issue First edition, and 28 pages).). Since Lynn-ized boron is the semi-conductor of a indirect transition mold, it is chiefly used for constituting stratum functionale other than a barrier layer with the component (Lynn-ized boron system semiconductor device) possessing the Lynn-ized boron system semi-conductor constituted considering Lynn-ized boron as a base material. It is in the Lynn-ized boron system semiconductor device, for example, a light emitting device, and the crystal layer which consists of a Lynn-ized boron semi-conductor is used as a contact (contact) layer (refer to JP,2-288388,A) for forming not a barrier layer (luminous layer) but a buffer coat (referring to U.S. Pat. No. 6,069,021 number), or an ohmic (Ohmic) nature electrode. Moreover, in the former, the example constituted as a substrate is indicated [single crystal / (silicon) / silicon (Si)] in these Lynn-ized boron system semi-conductor light emitting devices (refer to the above-mentioned U.S. Pat. No. 6,069,021 number).
[0003] it is in the conventional compound semiconductor light emitting device, and it comes out of a barrier layer (luminous layer) chiefly to consist of group-III-V-semiconducter crystal layers of a direct transition mold. For example, the barrier layer of near-ultraviolet, blue, green light emitting diode (LED), or a laser diode (LD) consists of gallium nitride indium (Ga1-YInYN:0 <=Y<=1) mixed crystal (refer to JP,55-3834,A). Even if it is in the Lynn-ized boron system semi-conductor light emitting device, the example which sets a luminous layer to Ga1-YInYN (0< Y<=1) is well-known (refer to the above-mentioned U.S. Pat. No. 6,069,021 number). It is in the conventional Lynn-ized boron system semi-conductor light emitting device, and the luminous layer which consists of Ga1-YInYN (0< Y<=1) is prepared on the crystal layer which consists for example, of Lynn-ized boron and indium (B1-XInXP:0 <=X<1) mixed crystal.
[0004] It is in the Lynn-ized boron system semi-conductor of a cubic sphalerite mold (zinc blende), for example, the lattice constant of the Lynn-ized boron (boron monophosphide:BP) of a monomer is 4.538A (refer to the above-mentioned "semiconductor device introduction" and 28 pages), and it excels in grid adjustment with the cubic gallium nitride (GaN) which makes a lattice constant 4.509A (refer to "Japanese crystal growth society magazine" Vol.25, No.3 (1998), and A 28 pages). For this reason, possibility of becoming suitable [Lynn-ized boron (BP)] as a substrate layer at the time of forming III group nitride semiconducting crystal layers, such as gallium nitride (GaN), is pointed out (refer to "Japanese crystal growth society magazine" Vol.26, and No. 2 (1999) or 29 pages).
[0005]
[Problem(s) to be Solved by the Invention] However, even if it is, for example, going to prepare the barrier layer which is made suitable to bring about luminescence of short wavelength from the former and which consists of Ga1-YInYN (0< Y<=1) on a Lynn-ized boron (BP) layer, it poses a problem that the Ga1-YInYN (0< Y<=1) crystal layer which makes an indium presentation (=Y) uniform in the increment direction of thickness is hard to be obtained. From the barrier layer which makes an indium presentation uneven in the direction of thickness, since luminescence which is excellent in high electron mobility or high monochromaticity cannot be obtained, the present condition is having caused trouble to obtaining the Lynn-ized boron system semiconductor device which is excellent in a property.
[0006] This invention is what was made that the trouble in the above-mentioned conventional technique should be solved. On the Lynn-ized boron system semiconducting crystal layer, the general formulas AlQGaRInYN, such as Ga1-YInYN (0< Y<=1) In preparing the barrier layer which consists of an III group nitride semiconducting crystal containing the indium (In) expressed with (0<=Q<1, 0<=R<1, 0< Y<=1, Q+R+Y=1), the technical means for obtaining a barrier layer with a uniform indium presentation is shown. [however,] Moreover, the Lynn-ized boron system semiconductor device which is excellent in an electric or optical property using this technical means is offered.
[0007]

[Means for Solving the Problem] Namely, the substrate with which this invention consists of a (1) silicon (Si) single crystal and the Lynn-ized boron system semiconducting crystal layer prepared on this substrate, With the interlayer who consists of a group-III-V-semiconducter crystal prepared on this Lynn-ized boron system semiconducting crystal layer The general formula AlQGaRInYN which sets to Y (0< Y<=1) the indium presentation established on this middle class In the Lynn-ized boron system semiconductor device equipped with the barrier layer which consists of an III group nitride semiconducting crystal expressed with (0<=Q<1, 0<=R<1, Q+R+Y=1) [however,] The Lynn-ized boron system semiconductor device characterized by being 1/2 or less [of an indium presentation (Y) of the III group nitride semiconducting crystal with which said middle class consists of a group-III-V-semiconducter crystal containing an indium, and this middle class's indium presentation makes said barrier layer].
(2) The Lynn-ized boron system semiconductor device given in the above (1) characterized by consisting of polycrystal layers which said interlayer turns into from the group-III-V-semiconducter crystal of the wurtzite mold (Wurtzite) containing the crystalline of a sphalerite mold (zinc blende).
(3) The Lynn-ized boron system semiconductor device given in the above (1) characterized by consisting of polycrystal layers which said interlayer turns into from the group-III-V-semiconducter crystal of the sphalerite mold containing the crystalline of a wurtzite mold.
(4) Said Lynn-ized boron system semiconducting crystal layer consists of Lynn-ized boron nitride and indium (BAInDN1-deltaPdelta:0<A<=1, 0<=D<1, A+D=1, 0< delta<=1) mixed crystal. said middle class -- an alumimium nitride gallium indium (aluminumgammaGabetaInalphaN: -- 0< alpha<=0.5, 0<=beta<1, and 0<=gamma<1 --) Alpha+beta+gamma = Consist of 1 mixed crystal and said barrier layer consists of alumimium nitride gallium indium (AlQGaRInYN:0<Y<=1, 0<=Q<1, 0<=R<1, Q+R+Y=1) mixed crystal. The above (1) characterized by being alpha<=0.5xY thru/or the Lynn-ized boron system semiconductor device given in (3).
(5) Said Lynn-ized boron system semiconducting crystal layer consists of Lynn-ized boron and indium (BAInDP:0<A<=1, 0<=D<1, A+D=1) mixed crystal. Said middle class consists of gallium nitride indium (GabetaInalphaN:0<alpha<=0.5, 0<=beta<1, alpha+beta = 1) mixed crystal. The Lynn-ized boron system semiconductor device given in the above (4) which a barrier layer consists of gallium nitride indium (GaRInYN:0<Y<=1, 0<=R<1, R+Y=1) mixed crystal, and is characterized by being alpha<=0.5xY.
(6) The above (1) which forms said interlayer by organic metal modified chemical vapor deposition (MOCVD law) thru/or the manufacture approach of the Lynn-ized boron system semiconductor device given in (5).
(7) The manufacture approach of the Lynn-ized boron system semiconductor device given in the above (6) which makes said interlayer's growth temperature 700 degrees C - 950 degrees C.
(8) Light emitting diode set to the above (1) thru/or (5) from the Lynn-ized boron system semiconductor device of a publication.
It comes out.
[0008]
[Embodiment of the Invention] In the 1st operation gestalt of this invention, the Lynn-ized boron system semiconducting crystal layer prepared on a silicon single crystal substrate is a layer which contains boron (B) and Lynn (P) as a configuration element, for example, consists of a BAAlBGaCInDP1-deltaAsdelta (0< A<=1, 0<=B<1, 0<=C<1, 0<=D<1, A+B+C+D=1, 0<=delta<1) crystal. Moreover, for example, it is the layer which consists of a BAAlBGaCInDP1-deltaNdelta (0< A<=1, 0<=B<1, 0<=C<1, 0<=D<1, A+B+C+D=1, 0<=delta<1) crystal. It is in the Lynn-ized boron system semi-conductor light emitting device, and the Lynn-ized boron system semiconducting crystal layer which consisted of large semiconducting crystals of a band gap rather than the barrier layer (luminous layer) can be used as a barrier layer to a barrier layer. Moreover, the Lynn-ized boron system semiconducting crystal layer of high resistance which added oxygen (O) etc. is in a field effect transistor (FET), controls leakage of the operating current from a barrier layer, and can use it as a buffer coat which is excellent in a mutual conductance (gm), for example.
[0009] The silicon single crystal (silicon) which has {100} sides, {110} sides, or {111} sides can be used for a substrate. The silicon single crystal which uses as a front face the crystal face which inclined in specific crystal orientation can also be used as a substrate. For example, the silicon single crystal which makes it an include angle and uses as a front face the {111} crystal faces which carried out the about 7 times (degree) inclination can be used for <110> crystal orientation as a substrate. It is in the Lynn-ized boron system semi-conductor light emitting device, and since positive/negative and which polar ohmic (Ohmic) nature electrode can be laid at the rear face of a substrate, then a substrate, n form or the silicon single crystal of p form conductivity can be contributed for constituting a light emitting device simple. The low conductive single crystal substrate of specific resistance (= resistivity) which makes resistivity especially more desirably less than [0.1mohm] contributes for bringing about LED with low forward voltage (the so-called Vf) below 1 milli ohm (mohms). Moreover, it becomes effective in constituting LD which brings about the oscillation stabilized since it excelled in heat dissipation nature. When are in the Lynn-ized boron system semi-conductor light emitting device, making it join to the silicon single crystal used as a substrate and preparing the Lynn-ized boron system semiconducting crystal layer, it is desirable to make the same the silicon single crystal of a substrate and conduction type of the Lynn-ized boron system semiconducting crystal layer.
[0010] The Lynn-ized boron system semiconducting crystal layer can be prepared through a buffer coat on the above-mentioned silicon single crystal substrate. Especially the buffer coat that consisted of Lynn-ized boron system semi-conductor layers of an amorphous substance or polycrystal eases stacking fault affinity

with the silicon single crystal which forms a substrate, and demonstrates effectiveness to bring about the Lynn-ized boron system semiconducting crystal layer with small crystal defect consistencies, such as a misfit rearrangement. Moreover, the boron which constitutes the buffer coat which consists of a Lynn-ized boron system semi-conductor layer, and Lynn demonstrate the operation as a "growth nucleus" which promotes growth, and take effect to bring about the Lynn-ized boron system semiconducting crystal layer which has a continuity on it. For example, the example which constitutes a buffer coat from Lynn-ized boron (BP) of the amorphous substance formed at the temperature of 250 degrees C - 750 degrees C by the MOCVD method or polycrystal can be given (refer to U.S. Pat. No. 6,069,021 number). As for the thickness of a buffer coat 102, it is desirable that it is referred to as 50nm or less by about 1nm or more, and it refers to to 15nm or less by 2 morenm or more.

[0011] On the Lynn-ized boron system semiconducting crystal layer, the interlayer who consists of a group-III-V-semiconducter crystal containing an indium is prepared. The description in the operation gestalt of **** 1 is to constitute the middle class from an III-V group ghost semiconducting crystal layer which has a specific indium presentation (=alpha). Although the middle class consists of group-III-V-semiconducter crystals, such as for example, a gallium nitride indium (Ga1-alphaInalphaN), the indium presentation (=alpha) is set to 0<alpha<=0.5xY. Y is an indium presentation (however, 0< Y<=1) of a barrier layer which consists of an III group nitride semiconducting crystal which is formed on an interlayer, and which is expressed with a general formula (however, 0<=Q<1, 0<=R<1, Q+R+Y=1) AlQGaRInYN here. If the barrier layer which has a uniform indium presentation for example, within a layer has the indium presentation (=Y) of the III group nitride semiconducting crystal layer which makes a barrier layer, it is the presentation itself. Moreover, if it is at the barrier layer which has inclination in the increment direction of thickness at an indium presentation, it is the indium presentation in the front face of the side which touches the middle class. Moreover, if it is in the barrier layer of the polyphase structure which consists of an aggregate of a crystal phase which is different in an indium presentation, it is the average of an indium presentation of each crystal phase.

[0012] It is prepared in order that especially the middle class of this invention may bring about the barrier layer which makes an indium presentation (=Y) uniform in the depth direction (the growth direction). It is stabilized and the barrier layer which has the indium presentation (=Y) of a uniform request in the depth direction as it is the high price for which the indium presentation (=alpha) of the group-III-V-semiconducter crystal layer which makes the middle class exceeds the mesial magnitude of an indium presentation (=Y) of the III group nitride semiconducting crystal which makes a barrier layer cannot be obtained. It originates in diffusion of the indium (In) atom from the middle class to a barrier layer side, and the barrier layer uneven in presentation to which the indium presentation (=Y) decreased is gradually concluded in the increment direction of the thickness of a barrier layer so that it may illustrate to drawing 1 especially. On the contrary, if the middle class is constituted from a group-III-V-semiconducter crystal layer which does not contain an indium (In), the barrier layer with which a desired indium presentation (=Y) is not filled will become being easy to conclude. The barrier layer uneven in presentation to which the indium presentation fell in the field by the side of the middle class of the deep part of a barrier layer is concluded so that it may illustrate to drawing 2 especially. Even if it uses the barrier layer which consists of an III group nitride semiconducting crystal with such an uneven indium presentation (=Y) as a luminous layer, various luminescence corresponding to change of an indium presentation (=Y) arises, and it does not come to obtain the Lynn-ized boron system semi-conductor light emitting device which brings about luminescence which is excellent in monochromaticity.

[0013] Moreover, on the interlayer exceeding the mesial magnitude (= 1/2) of an indium presentation (=Y) of an indium presentation (=alpha) of a barrier layer, the barrier layer which is excellent in surface surface smoothness can be stabilized, and cannot be formed. If alpha exceeds 0.5xY, irregularity will become rapidly remarkable on the surface of a barrier layer. A smooth junction interface cannot consist of barrier layers of the front face were rudely ruined. Even if it means the thing which use as an electronic transit layer (channel layer) the barrier layer which follows, for example, has such a coarse front face and for which it has hetero (different species) junction structure, uses, and the high mobility FET is constituted, the interior of the channel (channel) layer near the heterojunction interface cannot be made to carry out localization of the two-dimensional electron efficiently, but two-dimensional electron gas FET (TEGFET) which is excellent in a mutual conductance (gm) is not obtained, but becomes inconvenient. As for the interlayer who uses for TEGFET, it is desirable to constitute from same conduction type as an electronic transit layer or a group-III-V-semiconducter crystal layer of high resistance. Moreover, the thickness of the interlayer who can use suitable for FET is 1/2 or less [of a barrier layer]. For example, thickness suitable as an interlayer about the barrier layer which sets thickness to 15nm is under 7.5nm. Furthermore, it is about 5nm or less preferably. Thickness does not come [therefore] to cover the whole front face of the Lynn-ized boron system semiconducting crystal layer of a substrate with the interlayer of less than about 1nm ultra-thin film to homogeneity, and serves as trouble by him obtaining the depth direction or the barrier layer which has a uniform indium presentation superficially.

[0014] As compared with the thickness of a barrier layer, the interlayer of excessive thickness may become the factor which causes trouble to improvement in the property of the Lynn-ized boron system semiconductor device. Many of groups III-V semiconducter for constituting an interlayer are semi-conductors of a direct transition mold (refer to the above-mentioned "semiconductor device introduction" and 28 pages). It follows, for example, is in the Lynn-ized boron system semi-conductor light emitting device, and, in addition to a

barrier layer, luminescence from an interlayer may occur secondarily according to the component operating current which flows into an interlayer. With the operation gestalt of **** 1, since it (=Y) of a barrier layer is making the indium presentation (=alpha) different even if it is, when it constitutes the middle class from same ingredient as a barrier layer, the wavelength of secondary luminescence from the middle class differs from the luminescence wavelength from the barrier layer for which it originally asks. Usually, since the reinforcement of secondary luminescence from an interlayer increases, it serves as trouble obtaining the Lynn-ized boron system semi-conductor light emitting device which is excellent in the monochromaticity of luminescence, so that an interlayer's thickness is made into size. If an interlayer's thickness is made or less [of the thickness of a barrier layer] into 1/2, the reinforcement of secondary luminescence will be reduced rapidly. The conduction type of the interlayer who uses for constituting a light emitting device is made in agreement with any of a barrier layer or the Lynn-ized boron system semiconducting crystal layer they are.

[0015] The barrier layer of this invention prepared on the middle class consists of III group nitride semiconducting crystals expressed with the general formula (however, 0<=Q<1, 0<=R<1, Q+R+Y=1) AlQGaRInYN which sets an indium presentation to Y (0< Y<=1). The barrier layer of the Lynn-ized boron system semiconductor device concerning this invention can also consist of quantum well (Quantum Well:QW) structures. For example, the crystal layer which consists of Ga1-YInYN (0< Y<=1) etc. the barrier layer prepared on the Lynn-ized boron system semi-conductor layer can also consist of the singles (Single QW:SQW) or multiplex (Multi QW:MQW) structures which it had as a well (well) layer. A barrier (barrier) layer can consist of an alumimium nitride gallium (aluminum1-XGaXN:0 <=X<=1), GaN1-deltaPdelta (0<=delta<=1), etc. If the barrier layer which this invention says is in quantum well structure, or it brings about luminescence, it is a well layer an electron runs. Therefore, even if it faces preparing the quantum structure on the Lynn-ized boron system semiconducting crystal layer, after preparing the middle class of this invention for example, on a barrier layer, there is an advantage to which forming a well layer then the depth direction, or the well layer (barrier layer) that makes an indium presentation (=Y) uniform superficially is brought.

[0016] The 2nd operation gestalt of this invention constitutes an interlayer from the polycrystal layer which consists of a group-III-V-semiconducter crystal which has the special crystal structure. That is, it constitutes from a polycrystal layer which consists of a group-III-V-semiconducter crystal of the wurtzite mold (Wurtzite) containing the crystalline of a sphalerite mold (zinc blende). It does not consist of crystals of a single crystal mold uniformly, and the crystal layer in which the crystal of such a different crystal mold is intermingled is called a polycrystal layer by this invention. For example, the middle class who prepares on the Lynn-ized boron system semiconducting crystal layer which consists of Lynn-ized boron (BP) of a monomer consists of polycrystal layers of the gallium nitride indium (Ga1-alphaInalphaN:0<alpha<=0.5xY) of the wurtzite mold containing the crystalline of a sphalerite mold. Since the Lynn-ized boron system semiconducting crystal generally has the crystal structure of a sphalerite mold, when it constitutes an interlayer from a crystal layer of a wurtzite mold, the operation which eases the lattice strain which originates in the coefficient of thermal expansion between the Lynn-ized boron system semiconducting crystal layer and an interlayer or the difference in a lattice constant, and is generated is acquired from the interlayer containing the crystalline of such a sphalerite mold. Moreover, an interlayer absorbs Lynn (P) diffused in a barrier layer side from the Lynn-ized boron system semiconducting crystal layer of the substrate at the time of membrane formation of a barrier layer, and takes effect to control the atomic concentration of Lynn (P) in a barrier layer.

[0017] The 3rd operation gestalt of this invention constitutes from the group-III-V-semiconducter crystal layer which has the crystal structure which is different from the above in an interlayer. That is, it constitutes from a polycrystal layer which consists of a group-III-V-semiconducter crystal of the sphalerite mold containing the crystalline of a wurtzite mold. For example, it constitutes from a polycrystal layer of the group III-V semiconducter of the sphalerite mold containing the crystalline which consists of a gallium nitride indium of a wurtzite mold. The interlayer who consists of polycrystal layers which consist of a group-III-V-semiconducter crystal of the sphalerite mold containing the crystalline of a wurtzite mold since an III group nitride semiconducting crystal is generally a wurtzite mold eases the lattice strain which originates in the coefficient of thermal expansion between the barrier layers which consist of an interlayer and an III group nitride semiconducting crystal, or the difference in a lattice constant, and is generated, and has the operation which brings about the barrier layer which is excellent in crystallinity. Moreover, an interlayer absorbs Lynn (P) diffused in a barrier layer side from the Lynn-ized boron system semiconducting crystal layer of the substrate at the time of membrane formation of a barrier layer, and takes effect to control the atomic concentration of Lynn (P) in a barrier layer.

[0018] The 4th operation gestalt of this invention constitutes the Lynn-ized boron system semiconducting crystal layer from the Lynn-ized boron nitride and indium (BAlnDN1-deltaPdelta:0<A<=1, 0<=D<1, A+D=1, 0< delta<=1) mixed crystal. The middle class who prepares on the Lynn-ized boron system semiconducting crystal layer is constituted from alumimium nitride gallium indium (aluminumgammaGabetaInalphaN:0<alpha<=0.5, 0<=beta<1, 0<=gamma<1, alpha+beta+gamma = 1) mixed crystal. And a barrier layer consists of alumimium nitride gallium indium (AlQGaRInYN:0<Y<=1, 0<=Q<1, 0<=R<1, Q+R+Y=1) mixed crystal. It is referred to as alpha<=0.5xY here. From the Lynn-ized boron nitride and indium mixed crystal, there is an advantage which can constitute the Lynn-ized boron system semiconducting crystal layer which carries out lattice matching to the silicon single crystal used as a substrate (refer to JP,2000-22211,A). Moreover, since alumimium nitride gallium indium mixed crystal is a kind of wideband gap (wide bandgap) ingredient, it can constitute a barrier

layer convenient for carrying out outgoing radiation of a near-untraviolet band light or the short wavelength visible band light. Moreover, it has the specified indium presentation (it is alpha<=0.5xY at alpha, however 0< alpha<=0.5). And the interlayer who consisted of alumimium nitride gallium indium (aluminumgammaGabetaInalphaN:0<alpha<=0.5, 0<=beta<1, 0<=gamma<1, alpha+beta+gamma = 1) mixed crystal which comes to contain the configuration element of a barrier layer While offering the "growth nucleus" in growth of a barrier layer and promoting membrane formation of a barrier layer, a barrier layer with a uniform indium presentation (=Y) can also be hung down.

[0019] Furthermore, the 5th operation gestalt of this invention constitutes the Lynn-ized boron system semiconducting crystal layer from Lynn-ized boron and indium (BAInDP:0<A<=1, 0<=D<1, A+D=1) mixed crystal. The middle class who prepares on the Lynn-ized boron system semiconducting crystal layer is constituted from gallium nitride indium (GabetaInalphaN:0<alpha<=0.5, 0<=beta<1, alpha+beta = 1) mixed crystal. A barrier layer consists of gallium nitride indium (GaRInYN:0<Y<=1, 0<=R<1, R+Y=1) mixed crystal. It is referred to as alpha<=0.5xY here. BAInDP mixed crystal has more few configuration elements, therefore can perform formation of the Lynn-ized boron system semiconducting crystal layer as it is simple. The Lynn-ized boron system semiconducting crystal layer used as the barrier layer (cladding layer) to a barrier layer (luminous layer) can consist of Lynn-ized boron (BP) crystal layers of the monomer which makes the band gap in a room temperature about 3eV order especially. Moreover, the buffer coat of for example, an FET application can consist of Lynn-ized boron (BP) crystal layers containing impurities, such as oxygen (O), of high resistance. Moreover, since whenever [mutual lattice mismatch] can be performed with smallness if constituted from the same ingredient as a barrier layer although an indium presentation differs in the middle class, a good barrier layer with low crystal defect consistencies, such as a misfit (misfit) rearrangement, can be constituted. Especially the interlayer that consists of a wurtzite mold crystal intermingled in the crystalline of a sphalerite mold can contribute for bringing about the barrier layer which is excellent in crystallinity with few crystal defect consistencies.

[0020] The interlayer who consists of a group-III-V-semiconducter crystal can form membranes like the Lynn-ized boron system semiconducting crystal layer or a barrier layer with growth means, such as organic metal modified chemical vapor deposition (MOCVD law). for example, boron triethyl (C2H5) (3B) / cyclopentadienyl indium (C5H5In) / phosphine (PH3) raw material system MOCVD -- it depends on law and membranes can be formed. an indium raw material, then a polymer(polymer)-ized reaction with PH3 control C5H5In which does not present strong Lewis acid nature to PH3 of the Lewis (Lewis) basicity -- having -- MOCVD under ordinary pressure (abbreviation atmospheric pressure) -- the interlayer who contains a good indium also by law can be formed (refer to Japan JP,2098388,B). It faces depending on the MOCVD method and forming the middle class, and the thickness can be controlled by the amount of supply and its supply time amount of a raw material of an III group configuration element, such as boron (B) to a silicon single crystal substrate top, and an indium (In). The middle class's indium presentation (=alpha) changes the rate of the ratio of concentration of the amount of supply of the indium raw material to the total amount of the amount of supply of an III group configuration element, and is adjusted. Moreover, an interlayer's carrier concentration depends on ****(ing) and choosing the ratio (the so-called V/III ratio) of the amount of supply of V group configuration element to the amount of supply of the raw material of an III group configuration element, or adds and (doping) adjusts an impurity intentionally. As an impurity suitable for obtaining the interlayer of n form, silicon (Si), tin (Sn), sulfur (S), a selenium (Se), a tellurium (Te), etc. can be illustrated. There are zinc (Zn), magnesium (Mg), carbon (C), etc. in the dopant (dopant) of p form.

[0021] By the MOCVD method, on the Lynn[which was prepared on the silicon single crystal substrate]-ized boron system semiconducting crystal layer which consists of a Lynn-ized boron (BP) crystal of a monomer, for example It faces forming the interlayer who consists of alumimium nitride gallium indium (aluminumgammaGabetaInalphaN:0<alpha<=0.5, 0<=beta<1, 0<=gamma<1, alpha+beta+gamma = 1) mixed crystal, and it is the range of about 750 degrees C - about 1200 degrees C, and, as for the Lynn-ized boron crystal layer, it is desirable to form membranes. At the elevated temperature exceeding about 1200 degrees C, the Lynn-ized boron crystal of the polymer of B6P and B13P2 grade is generated, and the homogeneous crystal layer which consists of Lynn-ized boron of a monomer is not obtained, but it is unsuitable. It is suitable that an interlayer forms membranes from it in [low-temperature] about 700 degrees C - about 950 degrees C. If the interlayer who makes an indium presentation (alpha) size makes membrane formation temperature low temperature, the interlayer of a flat front face will be obtained. In order to form the interlayer who consists of an III group nitride semiconducting crystal layer containing aluminum (aluminum), it is suitable to make membrane formation temperature into an elevated temperature comparatively in the above-mentioned temperature requirement. Although an indium presentation is different, when the barrier layer which carries out a laminating on the middle class is constituted from same crystal ingredient, there is an advantage which can form a barrier layer simple at the temperature of an abbreviation EQC with the middle class. The indium presentation (alpha or Y) of the middle class or a barrier layer can carry out a quantum using component-analysis means, such as an X-ray diffraction method, a secondary ion mass spectrometry (SIMS), and the Auger (Auger) spectral-analysis method (AES).

[0022]

[Function] The middle class who has the indium presentation which was established in the middle with the barrier layer which consists of a silicon single crystal substrate and an III group nitride semiconducting crystal

layer containing an indium, and which was specified based on the indium presentation of a barrier layer has the operation which makes the indium presentation of a barrier layer equalize. Moreover, it has the operation which brings about the barrier layer which is excellent in surface surface smoothness.
[0023] Moreover, the interlayer who consists of a polycrystal layer containing the crystalline which has the indium presentation specified based on the indium presentation of a barrier layer, and is different in a crystal mold has the operation which brings about the barrier layer which is excellent in crystallinity.
[0024]
[Example] It mentions to the example which produced the light emitting diode (LED) which consists of a Lynn-ized boron system semiconductor device, and the contents of this invention are explained concretely. The mimetic diagram of LED1B concerning this example is shown in drawing 3 . Moreover, the cross section of LED1B in alignment with broken-line X-X' shown in drawing 3 is shown in drawing 4 .
[0025] Laminating structure 1A of an LED1B application constituted Si single crystal of p form which added the boron (B) which uses the crystal face (111) as a front face as a substrate 101. a substrate 101 top -- boron triethyl (C2H5) (3B) / phosphine (PH3) / hydrogen (H2) system ordinary pressure MOCVD -- the buffer coat 102 which consists of Lynn-ized boron which makes an amorphous substance a subject in the state of as-grown at 350 degrees C by law was deposited. The thickness of a buffer coat 102 could be about 10nm. The laminating of the Lynn-ized boron system semiconducting crystal layer 103 which consists of a monomer Lynn-ized boron (BP) crystal of p form where it was made to grow up at 1050 degrees C was carried out to the front face of a buffer coat 102 using the above-mentioned MOCVD vapor growth means. Carrier concentration of the Lynn-ized boron system semiconducting crystal layer 103 of p form was set to abbreviation 7x1018cm-3, and thickness could be about 400nm. The band gap in the room temperature of BP layer of the monomer which makes the Lynn-ized boron system semiconducting crystal layer 103 of p form was 3.0eV about.
[0026] the Lynn-ized boron system semiconducting crystal layer 103 top of p form -- trimethylgallium (CH3) (3Ga) / cyclopentadienyl indium (C5H5In) / ammonia (NH3) / H-2 system ordinary pressure MOCVD -- the laminating of the interlayer 104 who consists of an n form gallium nitride indium (Ga0.94In0.06N) of the wurtzite crystal mold which sets an indium presentation to 0.06 (= 6%) by law was carried out. An interlayer's 104 membrane formation temperature was made into 800 degrees C, and thickness could be 15nm. From the cross-section TEM image using a transmission electron microscope (TEM), and the limit visual field electron diffraction graphic form, existence of crystalline 104a of a sphalerite mold was checked inside the interlayer 104. Crystalline 104a existed to the field near the junction interface with the Lynn-ized boron system semiconducting crystal layer 103 mostly especially. The magnitude of crystalline 104a was about 2nm to about 5nm in general.
[0027] On the middle class's 104 front face, the barrier layer (luminous layer) 105 which consists of a Wuts ore type (Silicon Si) dope n form gallium nitride indium (Ga0.85In0.15N) which sets an indium presentation to 0.15 (= 15%) was deposited. Membrane formation temperature of a barrier layer 105 was made into 800 degrees C as well as the interlayer 104, and thickness could be about 300nm. Moreover, the carrier concentration of a barrier layer 105 was set as abbreviation 6x1017cm-3. Distribution of the depth direction of an indium presentation of the barrier layer 105 interior which depended on the secondary ion mass spectrometry (SIMS), and was measured was as uniform as about 0.15 until it resulted in the junction interface with an interlayer 104, as shown in drawing 5 . An interlayer's 104 capture operation over the Lynn (P) atom which the concentration of the Lynn (P) atom in the contrant region of the barrier layer 105 near the junction interface with an interlayer 104 is less than [about 1x1018cm -] three, and is diffused from the Lynn-ized boron system semiconducting crystal layer 103 of p form had manifested itself. Moreover, in observation by cross-section TEM technique, most rearrangements penetrated in a barrier layer 105 from the Lynn-ized boron system semi-conductor layer 103 were not checked by looking.
[0028] On the barrier layer 105, the laminating of the Lynn-ized boron system semiconducting crystal layer 106 of n form which consists of Lynn-ized boron (BP) of a monomer was carried out. Carrier concentration of the Lynn-ized boron system semiconducting crystal layer 106 of n form was set to abbreviation 1x1019cm-3, and thickness could be about 400nm. The Lynn-ized boron system semiconducting crystal layer 106 of n mold constituted the band gap in a room temperature from a Lynn-ized boron crystal of a monomer set to 3.0eV about. n -- a form -- Lynn ---izing -- boron -- a system -- a semiconducting crystal -- a layer -- 106 -- and -- p -- a form -- Lynn ---izing -- boron -- a system -- a semiconducting crystal -- a layer -- 103 -- a barrier layer -- 105 -- from -- the middle class -- 104 -- p -- a form -- Lynn ---izing -- boron -- a system -- a semiconducting crystal -- a layer -- 103 -- pn junction -- structure -- having had -- double -- a hetero -- (-- DH --) -- structure -- a light-emitting part -- having constituted .
[0029] In the center section of the front face of the Lynn-ized boron system semiconducting crystal layer 106 of n form, the surface ohmic electrode 107 of the three-tiered structure which serves as the plinth electrode for connection has been arranged. The surface ohmic electrode 107 set the diameter to about 120 micrometers, and made it circular. Part 107a in contact with n form Lynn-ized boron semiconducting crystal layer 106 of the surface ohmic electrode 107 consisted of vacuum deposition film (thickness **700nm) of golden (Au) and a germanium (germanium) alloy. On Au-germanium vacuum deposition film 107a, nickel (nickel) vacuum deposition film (thickness **100nm) 107b covering of was done. Au vacuum deposition film (thickness **1000nm) 107c was made to put on nickel vacuum deposition film 107b. On the other hand, the conductivity

of the p form Si single crystal substrate 101 was utilized, and the rear-face ohmic electrode 108 which consists of (Aluminum aluminum) vacuum deposition film (thickness **700nm) has been arranged all over the abbreviation for the rear face of a substrate 101. Then, laminating structure 1A was judged along the direction parallel to the <211> crystal orientation of Si single crystal of a substrate 101, and perpendicular, and it was referred to as LED1B of the square which sets one side to about 350 micrometers.
[0030] Between the surface ohmic electrode 107 and the rear-face ohmic electrode 108, conduction of the operating current of 20mA (mA) was carried out to the forward direction, and the luminescence property of LED1B was investigated. Emission center wavelength was set to 460nm. The middle class's 104 indium presentation (= 0.06) was written below in the mesial magnitude (= 1/2) of an indium presentation (= 0.15) of a barrier layer 105, and luminescence secondary in addition to this main emission spectrum was not accepted, but luminescence was what is excellent in the monochromaticity which sets half-value width (=FWHM) to about 20nm. Moreover, according to an operation of the interlayer 104 who consists of a configuration containing the crystalline from which a crystal mold is different, since the barrier layer 105 with few penetration rearrangements was brought about, the brightness measured in the state of a chip (chip) using a common integrating sphere became a 9mm candela (mcd). Moreover, the forward voltage (Vf) called for from the usual current-electrical-potential-difference (I-V) property was about 3.7V (forward current = 20mA). Moreover, the reverse voltage (Vr) which is an electrical potential difference at the time of a reverse current reaching 10microA is about 10v or more, and the good pn junction property (rectifying characteristic) manifested itself. As mentioned above, a result provided with the Lynn-ized boron system semi-conductor LED which is excellent in pressure resistance was brought, presenting high luminescence reinforcement to this invention therefore.
[0031]
[Effect of the Invention] The substrate which consists of a silicon single crystal, and the Lynn-ized boron system semiconducting crystal layer prepared on the substrate, With the interlayer who turns into a substrate layer of the barrier layer prepared on the Lynn-ized boron system semiconducting crystal layer It faces constituting the Lynn-ized boron system semiconductor device using the barrier layer which consists of an III group nitride semiconducting crystal which sets an indium presentation to Y (0< Y<=1) on the middle class. In this invention Since an interlayer is constituted from a group III-V semiconducter of 1/2 or less indium presentation of an indium presentation of an III group nitride semiconducting crystal layer who makes a barrier layer For example, it is in the Lynn-ized boron system semi-conductor light emitting devices, such as LED, secondary luminescence which disturbs the monochromaticity of luminescence can be avoided, and effect is taken to bring about the light emitting device which is excellent in monochromaticity.
[0032] Moreover, in this invention, since the middle class was constituted from a polycrystal layer containing the crystalline to which a crystal mold is different from making the middle class's indium presentation or less [which makes a barrier layer / of an indium presentation of an III group nitride semiconducting crystal layer] into 1/2 in addition, the light emitting diode which consists of a Lynn-ized boron system semiconductor device which is excellent in luminescence reinforcement and an electric proof-pressure property, for example has been offered.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing distribution of an indium presentation of the depth direction of a barrier layer when the middle class's indium presentation is high.
[Drawing 2] It is drawing showing distribution of an indium presentation of the depth direction of a barrier layer in case the middle class does not contain an indium.
[Drawing 3] It is the mimetic diagram of LED concerning the example of this invention.
[Drawing 4] It is the cross section of LED in alignment with broken-line X-X' shown in drawing 3 .
[Drawing 5] It is drawing showing distribution of an indium presentation of the depth direction of the barrier layer concerning the example of this invention.
[Description of Notations]
1A Light emitting device (LED) application laminating structure
1B LED
101 Substrate
102 Buffer Coat
103 Lynn-ized Boron System Semiconducting Crystal Layer of P Form
104 Interlayer
104a Crystalline
105 Barrier Layer
106 Lynn-ized Boron System Semiconducting Crystal Layer of N Form
107 Surface Ohmic Electrode
107a Au-germanium vacuum deposition film
107b nickel vacuum deposition film
107c Au vacuum deposition film
108 Rear-Face Ohmic Electrode

[Translation done.]

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(71)出願人　000002004
昭和電工株式会社
東京都港区芝大門１丁目13番９号
(72)発明者　宇田川　隆
埼玉県秩父市大字下影森1505番地　昭和電工株式会社総合研究所秩父研究室内
(74)代理人　100118740
弁理士　柿沼　伸司

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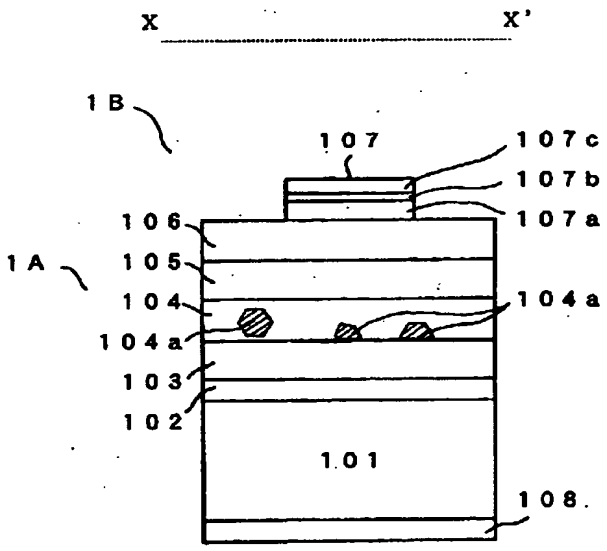
(54)【発明の名称】　リン化硼素系半導体素子、その製造方法、および発光ダイオード

(57)【要約】
【課題】リン化硼素系半導体結晶層上に、一般式ＡｌQＧａRＩｎγＮ（但し、０≦Ｑ＜１、０≦Ｒ＜１、０＜Ｙ≦１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるインジウム（Ｉｎ）を含有するＩＩＩ族窒化物半導体結晶からなる活性層を設けるにあたり、インジウム組成が均一な活性層を得るための技術手段を提示する。
【解決手段】活性層をなすＩＩＩ族窒化物半導体結晶層のインジウム組成の１／２以下のインジウム組成を有するＩＩＩ－Ｖ族化合物半導体からなる中間層をリン化硼素系半導体結晶層と活性層との間に設ける。結晶型の相違する結晶体を含む多結晶層から中間層を構成する。



【特許請求の範囲】
【請求項１】珪素（Ｓｉ）単結晶からなる基板と、該基板上に設けられたリン化硼素系半導体結晶層と、該リン化硼素系半導体結晶層上に設けられたＩＩＩ－Ｖ族化合物半導体結晶からなる中間層と、該中間層上に設けられたインジウム組成をＹ（０＜Ｙ≦１）とする一般式$A_IQGaRInγN$（但し、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるＩＩＩ族窒化物半導体結晶からなる活性層とを備えたリン化硼素系半導体素子に於いて、前記中間層がインジウムを含有するＩＩＩ－Ｖ族化合物半導体結晶からなり、該中間層のインジウム組成が前記活性層をなすＩＩＩ族窒化物半導体結晶のインジウム組成（Ｙ）の１／２以下であることを特徴とするリン化硼素系半導体素子。
【請求項２】前記中間層が、閃亜鉛鉱型（ｚｉｎｃ　ｂｌｅｎｄｅ）の結晶体を含むウルツ鉱型（Ｗｕｒｔｚｉｔｅ）のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成されることを特徴とする請求項１に記載のリン化硼素系半導体素子。
【請求項３】前記中間層が、ウルツ鉱型の結晶体を含む閃亜鉛鉱型のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成されることを特徴とする請求項１に記載のリン化硼素系半導体素子。
【請求項４】前記リン化硼素系半導体結晶層がリン化窒化硼素・インジウム（$B_AInDN_{1-δ}Pδ$：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１、０＜$δ$≦１）混晶から構成され、前記中間層が窒化アルミニウム・ガリウム・インジウム（$AlγGaβInαN$：０＜$α$≦０．５、０≦$β$＜１、０≦$γ$＜１、、$α$＋$β$＋$γ$＝１）混晶から構成され、前記活性層が窒化アルミニウム・ガリウム・インジウム（$A_IQGaRInγN$：０＜Ｙ≦１、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）混晶から構成され、$α$≦０．５×Ｙであることを特徴とする請求項１乃至３に記載のリン化硼素系半導体素子。
【請求項５】前記リン化硼素系半導体結晶層がリン化硼素・インジウム（B_AInDP：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１）混晶から構成され、前記中間層が窒化ガリウム・インジウム（$GaβInαN$：０＜$α$≦０．５、０≦$β$＜１、$α$＋$β$＝１）混晶から構成され、活性層が窒化ガリウム・インジウム（$GaRInγN$：０＜Ｙ≦１、０≦Ｒ＜１、Ｒ＋Ｙ＝１）混晶から構成され、$α$≦０．５×Ｙであることを特徴とする請求項４に記載のリン化硼素系半導体素子。
【請求項６】前記中間層を有機金属化学的気相堆積法（ＭＯＣＶＤ法）で成膜する請求項１ないし５に記載のリン化硼素系半導体素子の製造方法。
【請求項７】前記中間層の成長温度を７００℃～９５０℃とする請求項６に記載のリン化硼素系半導体素子の製造方法。
【請求項８】請求項１ないし５に記載のリン化硼素系半導体素子からなる発光ダイオード。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、リン化硼素系半導体結晶層上に活性層を備えてなるリン化硼素系半導体素子を構成するための技術に係わり、特に、素子特性の向上をもたらす組成の均一性に優れた活性層を構成するための技術に関する。
【０００２】
【従来の技術】従来より、一種のＩＩＩ－Ｖ族化合物半導体としてリン化硼素（ＢＰ）が知られている（寺本巌著、「半導体デバイス概論」（１９９５年３月３０日、（株）培風館発行初版、２８頁参照）。リン化硼素は、間接遷移型の半導体であるため、リン化硼素を基材として構成されるリン化硼素系半導体を具備する素子（リン化硼素系半導体素子）では、活性層以外の機能層を構成するにもっぱら利用されている。リン化硼素系半導体素子、例えば発光素子にあって、リン化硼素半導体からなる結晶層は、活性層（発光層）ではなく、緩衝層（米国特許６，０６９，０２１号参照）或いはオーミック（Ｏｈｍｉｃ）性電極を形成するためのコンタクト（ｃｏｎｔａｃｔ）層（特開平２－２８８３８８号公報参照）として利用されている。また、従来では、これらのリン化硼素系半導体発光素子を珪素（Ｓｉ）単結晶（シリコン）を基板として構成する例が開示されている（上記の米国特許６，０６９，０２１号参照）。
【０００３】従来の化合物半導体発光素子にあって、活性層（発光層）は直接遷移型のＩＩＩ－Ｖ族化合物半導体結晶層から構成されるのがもっぱらである。例えば、近紫外、青色或いは緑色発光ダイオード（ＬＥＤ）或いはレーザダイオード（ＬＤ）の活性層は、窒化ガリウム・インジウム（$Ga_{1-γ}InγN$：０≦Ｙ≦１）混晶から構成されている（特開昭５５－３８３４号公報参照）。リン化硼素系半導体発光素子にあっても、発光層を$Ga_{1-γ}InγN$（０＜Ｙ≦１）とする例が公知となっている（上記の米国特許６，０６９，０２１号参照）。従来のリン化硼素系半導体発光素子にあって、$Ga_{1-γ}InγN$（０＜Ｙ≦１）からなる発光層は例えば、リン化硼素・インジウム（$B_{1-χ}InχP$：０≦Ｘ＜１）混晶からなる結晶層上に設けられている。
【０００４】立方晶の閃亜鉛鉱型（ｚｉｎｃ　ｂｌｅｎｄｅ）のリン化硼素系半導体にあって、例えば、単量体のリン化硼素（ｂｏｒｏｎ　ｍｏｎｏｐｈｏｓｐｈｉｄｅ：ＢＰ）の格子定数は４．５３８Åであり（上記の「半導体デバイス概論」、２８頁参照）、格子定数を４．５０９Åとする立方晶の窒化ガリウム（ＧａＮ）との格子整合性に優れている（「日本結晶成長学会誌」、Ｖｏｌ．２５，Ｎｏ．３（１９９８）、Ａ２８頁参照）。このため、リン化硼素（ＢＰ）は、窒化ガリウム（ＧａＮ）等のＩＩＩ族窒化物半導体結晶層を形成する

際の下地層として好適となる可能性が指摘されている（「日本結晶成長学会誌」、Ｖｏｌ．２６，Ｎｏ．２（１９９９）、２９頁参照）。

【０００５】

【発明が解決しようとする課題】しかしながら、従来から短波長の発光をもたらすに好適とされる例えば、$Ga_{1-Y}In_YN$（０＜Ｙ≦１）からなる活性層をリン化硼素（ＢＰ）層上に設けようとしても、層厚の増加方向にインジウム組成（＝Ｙ）を均一とする$Ga_{1-Y}In_YN$（０＜Ｙ≦１）結晶層が得られ難いことが問題となっている。インジウム組成を層厚方向で不均一とする活性層からは高い電子移動度或いは単色性に優れる発光を得ることはできないため、特性に優れるリン化硼素系半導体素子を得るに支障を来しているのが現状である。

【０００６】本発明は、上記の従来技術に於ける問題点を解決すべくなされたもので、リン化硼素系半導体結晶層上に、$Ga_{1-Y}In_YN$（０＜Ｙ≦１）等の一般式$Al_QGa_RIn_YN$（但し、０≦Ｑ＜１、０≦Ｒ＜１、０＜Ｙ≦１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるインジウム（Ｉｎ）を含有するＩＩＩ族窒化物半導体結晶からなる活性層を設けるにあたり、インジウム組成が均一な活性層を得るための技術手段を提示するものである。また、この技術手段を利用して電気的或いは光学的な特性に優れるリン化硼素系半導体素子を提供するものである。

【０００７】

【課題を解決するための手段】即ち、本発明は

（１）珪素（Ｓｉ）単結晶からなる基板と、該基板上に設けられたリン化硼素系半導体結晶層と、該リン化硼素系半導体結晶層上に設けられたＩＩＩ－Ｖ族化合物半導体結晶からなる中間層と、該中間層上に設けられたインジウム組成をＹ（０＜Ｙ≦１）とする一般式$Al_QGa_RIn_YN$（但し、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるＩＩＩ族窒化物半導体結晶からなる活性層とを備えたリン化硼素系半導体素子に於いて、前記中間層がインジウムを含有するＩＩＩ－Ｖ族化合物半導体結晶からなり、該中間層のインジウム組成が前記活性層をなすＩＩＩ族窒化物半導体結晶のインジウム組成（Ｙ）の１／２以下であることを特徴とするリン化硼素系半導体素子。

（２）前記中間層が、閃亜鉛鉱型（ｚｉｎｃ　ｂｌｅｎｄｅ）の結晶体を含むウルツ鉱型（Ｗｕｒｔｚｉｔｅ）のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成されることを特徴とする上記（１）に記載のリン化硼素系半導体素子。

（３）前記中間層が、ウルツ鉱型の結晶体を含む閃亜鉛鉱型のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成されることを特徴とする上記（１）に記載のリン化硼素系半導体素子。

（４）前記リン化硼素系半導体結晶層がリン化窒化硼素・インジウム（$B_AIn_DN_{1-\delta}P_\delta$：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１、０＜$\delta$≦１）混晶から構成され、前記中間層が窒化アルミニウム・ガリウム・インジウム（$Al_\gamma Ga_\beta In_\alpha N$：０＜$\alpha$≦０．５、０≦$\beta$＜１、０≦$\gamma$＜１、、$\alpha+\beta+\gamma=1$）混晶から構成され、前記活性層が窒化アルミニウム・ガリウム・インジウム（$Al_QGa_RIn_YN$：０＜Ｙ≦１、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）混晶から構成され、α≦０．５×Ｙであることを特徴とする上記（１）乃至（３）に記載のリン化硼素系半導体素子。

（５）前記リン化硼素系半導体結晶層がリン化硼素・インジウム（B_AIn_DP：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１）混晶から構成され、前記中間層が窒化ガリウム・インジウム（$Ga_\beta In_\alpha N$：０＜α≦０．５、０≦β＜１、$\alpha+\beta=1$）混晶から構成され、活性層が窒化ガリウム・インジウム（Ga_RIn_YN：０＜Ｙ≦１、０≦Ｒ＜１、Ｒ＋Ｙ＝１）混晶から構成され、α≦０．５×Ｙであることを特徴とする上記（４）に記載のリン化硼素系半導体素子。

（６）前記中間層を有機金属化学的気相堆積法（ＭＯＣＶＤ法）で成膜する上記（１）ないし（５）に記載のリン化硼素系半導体素子の製造方法。

（７）前記中間層の成長温度を７００℃～９５０℃とする上記（６）に記載のリン化硼素系半導体素子の製造方法。

（８）上記（１）ないし（５）に記載のリン化硼素系半導体素子からなる発光ダイオード。

である。

【０００８】

【発明の実施の形態】本発明の第１の実施形態に於いて、珪素単結晶基板上に設けるリン化硼素系半導体結晶層は、硼素（Ｂ）とリン（Ｐ）とを構成元素として含む、例えば、$B_AAl_BGa_CIn_DP_{1-\delta}As_\delta$（０＜Ａ≦１、０≦Ｂ＜１、０≦Ｃ＜１、０≦Ｄ＜１、Ａ＋Ｂ＋Ｃ＋Ｄ＝１、０≦δ＜１）結晶からなる層である。また、例えば、$B_AAl_BGa_CIn_DP_{1-\delta}N_\delta$（０＜Ａ≦１、０≦Ｂ＜１、０≦Ｃ＜１、０≦Ｄ＜１、Ａ＋Ｂ＋Ｃ＋Ｄ＝１、０≦δ＜１）結晶からなる層である。リン化硼素系半導体発光素子にあって、活性層（発光層）よりも禁止帯幅の広い半導体結晶から構成されたリン化硼素系半導体結晶層は活性層に対する障壁層として利用できる。また、例えば、酸素（Ｏ）等を添加した高抵抗のリン化硼素系半導体結晶層は、例えば、電界効果型トランジスタ（ＦＥＴ）にあって、活性層からの動作電流の漏洩を抑制し、相互コンダクタンス（g_m）に優れる緩衝層として利用できる。

【０００９】基板には、｛１００｝面、｛１１０｝面、或いは｛１１１｝面を有する珪素単結晶（シリコン）を利用できる。特定の結晶方向に傾斜した結晶面を表面とする珪素単結晶も、基板として利用できる。例えば、＜１１０＞結晶方向に角度にして約７度（°）傾斜した

【１１１】結晶面を表面とする珪素単結晶を基板として利用できる。リン化硼素系半導体発光素子にあって、ｎ形またはｐ形伝導性の珪素単結晶を基板とすれば、基板の裏面に正負、何れかの極性のオーミック（Ｏｈｍｉｃ）性電極を敷設できるため、簡便に発光素子を構成するに寄与できる。特に、抵抗率を１ミリオーム（ｍΩ）以下、より望ましくは０．１ｍΩ以下とする低い比抵抗（＝抵抗率）の導電性単結晶基板は、順方向電圧（所謂、Ｖｆ）の低いＬＥＤをもたらすに貢献する。また、放熱性に優れるため安定した発振をもたらすＬＤを構成するに有効となる。リン化硼素系半導体発光素子にあって、基板とする珪素単結晶に接合させてリン化硼素系半導体結晶層を設ける場合、基板の珪素単結晶とリン化硼素系半導体結晶層の伝導形を同一とするのが望ましい。

【００１０】リン化硼素系半導体結晶層は、上記の珪素単結晶基板上に緩衝層を介して設けることができる。特に、非晶質または多結晶のリン化硼素系半導体層から構成された緩衝層は、基板をなす珪素単結晶との格子不整合性を緩和して、ミスフィット転位等の結晶欠陥密度の小さいリン化硼素系半導体結晶層をもたらすに効果を発揮する。また、リン化硼素系半導体層からなる緩衝層を構成する硼素とリンは、成長を促進する「成長核」としての作用を発揮し、その上に連続性のあるリン化硼素系半導体結晶層をもたらすに効果を奏する。例えば、ＭＯＣＶＤ法により２５０℃～７５０℃の温度で形成した非晶質または多結晶のリン化硼素（ＢＰ）から緩衝層を構成する例を挙げられる（米国特許６，０６９，０２１号参照）。緩衝層１０２の層厚は約１ｎｍ以上で５０ｎｍ以下、更には２ｎｍ以上で１５ｎｍ以下とするのが好ましい。

【００１１】リン化硼素系半導体結晶層上には、インジウムを含有するＩＩＩ－Ｖ族化合物半導体結晶からなる中間層を設ける。本第１の実施形態に於ける特徴は、中間層を特定のインジウム組成（＝α）を有するＩＩＩ－Ｖ族化物半導体結晶層から構成していることにある。中間層は例えば、窒化ガリウム・インジウム（$Ga_{1-\alpha}In_{\alpha}N$）等のＩＩＩ－Ｖ族化合物半導体結晶から構成するが、そのインジウム組成（＝α）は、０＜α≦０．５×Ｙとする。ここでＹは、中間層の上に形成される、一般式$Al_{Q}Ga_{R}In_{Y}N$（但し、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるＩＩＩ族窒化物半導体結晶からなる活性層のインジウム組成（但し０＜Ｙ≦１）である。活性層をなすＩＩＩ族窒化物半導体結晶層のインジウム組成（＝Ｙ）とは、例えば、層内で均一なインジウム組成を有する活性層にあっては、その組成そのものである。また、層厚の増加方向にインジウム組成に勾配を有する活性層にあっては、中間層と接する側の表面に於けるインジウム組成である。また、インジウム組成を相違する結晶相の集合体からなる多相構造の活性層にあっては、各結晶相のインジウム組成の平均値である。

【００１２】本発明の中間層は、特に深さ方向（成長方向）にインジウム組成（＝Ｙ）を均一とする活性層をもたらすために設けられるものである。中間層をなすＩＩＩ－Ｖ族化合物半導体結晶層のインジウム組成（＝α）が活性層をなすＩＩＩ族窒化物半導体結晶のインジウム組成（＝Ｙ）の半値を越える高値であると、深さ方向に均一な所望のインジウム組成（＝Ｙ）を有する活性層を安定して得ることができない。特に、図１に例示する如く、中間層から活性層側へのインジウム（Ｉｎ）原子の拡散に起因して、活性層の層厚の増加方向に漸次、インジウム組成（＝Ｙ）が減少した組成的に不均一な活性層が帰結される。逆に、中間層をインジウム（Ｉｎ）を含まないＩＩＩ－Ｖ族化合物半導体結晶層から構成すると、所望のインジウム組成（＝Ｙ）に満たない活性層が帰結され易くなる。特に、図２に例示する様に、活性層の深部の中間層側の領域に於いてインジウム組成が低下した組成的に不均一な活性層が帰結される。この様なインジウム組成（＝Ｙ）の不均一なＩＩＩ族窒化物半導体結晶からなる活性層を発光層として利用しても、インジウム組成（＝Ｙ）の変化に対応した種々の発光が生じ、単色性に優れる発光をもたらすリン化硼素系半導体発光素子を得るに至らない。

【００１３】また、インジウム組成（＝α）を、活性層のインジウム組成（＝Ｙ）の半値（＝１／２）を越えるものとする中間層上には、表面の平坦性に優れる活性層を安定して形成できない。αが０．５×Ｙを越えると、活性層の表面に凹凸が急激に顕著となる。粗雑に荒れた表面の活性層では、平滑な接合界面を構成できない。従って、例えば、この様な粗雑な表面を有する活性層を電子走行層（チャネル層）とするヘテロ（異種）接合構造して利用して高移動度ＦＥＴを構成することを意図しても、ヘテロ接合界面の近傍のチャネル（ｃｈａｎｎｅｌ）層の内部に効率的に２次元電子を局在させることができず、相互コンダクタンス（g_m）に優れる２次元電子ガスＦＥＴ（ＴＥＧＦＥＴ）は得られず不都合となる。ＴＥＧＦＥＴに利用する中間層は、電子走行層と同一の伝導形或いは高抵抗のＩＩＩ－Ｖ族化合物半導体結晶層から構成するのが望ましい。また、ＦＥＴに好適に利用できる中間層の層厚は活性層の１／２以下である。例えば、層厚を１５ｎｍとする活性層について、中間層として好適な層厚は７．５ｎｍ下である。更に、好ましくは約５ｎｍ以下である。層厚が約１ｎｍ未満の極薄膜の中間層では、下地のリン化硼素系半導体結晶層の表面全体を均一に被覆するに至らず、従って、深さ方向或いは平面的に均一なインジウム組成を有する活性層を得るに支障となる。

【００１４】活性層の層厚に比較して過大である層厚の中間層は、リン化硼素系半導体素子の特性の向上に支障を来す要因となる場合がある。中間層を構成するための

ＩＩＩ－Ｖ族化合物半導体の多くは直接遷移型の半導体である（上記の「半導体デバイス概論」、２８頁参照）。従って、例えば、リン化硼素系半導体発光素子にあって、中間層に流入する素子動作電流によって、活性層に加え中間層からの発光が副次的に発生してしまう場合がある。本第１の実施形態では、中間層を活性層と同一の材料から構成する場合にあっても、インジウム組成（＝α）は活性層のそれ（＝Ｙ）とは相違させているので、中間層からの副次的な発光の波長は、本来所望する活性層からの発光波長とは異なるものとなる。通常、中間層の層厚を大とする程、中間層からの副次的な発光の強度は増大するため、発光の単色性に優れるリン化硼素系半導体発光素子を得るに支障となる。中間層の層厚を、活性層の層厚の１／２以下とすると副次的な発光の強度は、急激に低下させられる。発光素子を構成するに利用する中間層の伝導形は、活性層またはリン化硼素系半導体結晶層の何れかと一致させる。

【００１５】中間層上に設ける本発明の活性層は、インジウム組成をＹ（０＜Ｙ≦１）とする一般式$A_{1Q}Ga_{R}In_{\gamma}N$（但し、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）で表わされるＩＩＩ族窒化物半導体結晶から構成する。本発明に係わるリン化硼素系半導体素子の活性層は、量子井戸（Ｑｕａｎｔｕｍ　Ｗｅｌｌ：ＱＷ）構造からも構成できる。例えば、リン化硼素系半導体層上に設ける活性層を、$Ga_{1-\gamma}In_{\gamma}N$（０＜Ｙ≦１）等からなる結晶層を井戸（ｗｅｌｌ）層として備えた単一（Ｓｉｎｇｌｅ　ＱＷ：ＳＱＷ）或いは多重（Ｍｕｌｔｉ　ＱＷ：ＭＱＷ）構造から構成することもできる。バリア（ｂａｒｒｉｅｒ）層は窒化アルミニウム・ガリウム（$Al_{1-\chi}Ga_{\chi}N$：０≦Ｘ≦１）や$GaN_{1-\delta}P_{\delta}$（０≦δ≦１）等から構成できる。本発明の云う活性層とは、量子井戸構造にあっては、発光をもたらす或いは電子が走行する井戸層である。従って、リン化硼素系半導体結晶層上に量子構造体を設けるに際しても、本発明の中間層を例えば、バリア層上に設けた後、井戸層を形成することとすれば、深さ方向或いは平面的にインジウム組成（＝Ｙ）を均一とする井戸層（活性層）がもたらされる利点がある。

【００１６】本発明の第２の実施形態では、中間層を特殊な結晶構造を有するＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成する。すなわち、閃亜鉛鉱型（ｚｉｎｃ　ｂｌｅｎｄｅ）の結晶体を含むウルツ鉱型（Ｗｕｒｔｚｉｔｅ）のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成する。単一の結晶型の結晶から画一的に構成されているのではなく、この様な異なる結晶型の結晶が混在している結晶層を本発明では多結晶層と称する。例えば、単量体のリン化硼素（ＢＰ）からなるリン化硼素系半導体結晶層上に設ける中間層を、閃亜鉛鉱型の結晶体を含むウルツ鉱型の窒化ガリウム・インジウム（$Ga_{1-\alpha}In_{\alpha}N$：０＜α≦０．５×Ｙ）の多結晶層から構成する。リン化硼素系半導体結晶は一般に閃亜鉛鉱型の結晶構造を有するため、ウルツ鉱型の結晶層から中間層を構成する場合、この様な閃亜鉛鉱型の結晶体を含む中間層からは、リン化硼素系半導体結晶層と中間層との間の熱膨張率或いは格子定数の差異等に起因して発生する格子歪を緩和する作用が得られる。また、中間層は、活性層の成膜時に於ける、下地のリン化硼素系半導体結晶層より活性層側に拡散して来るリン（Ｐ）を吸収して、活性層内のリン（Ｐ）の原子濃度を抑制するに効果を奏する。

【００１７】本発明の第３の実施形態では、また中間層を上記とは異なる結晶構造を有するＩＩＩ－Ｖ族化合物半導体結晶層から構成する。すなわち、ウルツ鉱型の結晶体を含む閃亜鉛鉱型のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成する。例えば、ウルツ鉱型の窒化ガリウム・インジウムからなる結晶体を含む閃亜鉛鉱型のＩＩＩ－Ｖ族化合物半導体の多結晶層から構成する。ＩＩＩ族窒化物半導体結晶は一般にウルツ鉱型であるため、ウルツ鉱型の結晶体を含む閃亜鉛鉱型のＩＩＩ－Ｖ族化合物半導体結晶からなる多結晶層から構成される中間層は、中間層とＩＩＩ族窒化物半導体結晶からなる活性層との間の熱膨張率或いは格子定数の差異等に起因して発生する格子歪を緩和して、結晶性に優れる活性層をもたらす作用を有する。また、中間層は、活性層の成膜時に於ける、下地のリン化硼素系半導体結晶層より活性層側に拡散して来るリン（Ｐ）を吸収して、活性層内のリン（Ｐ）の原子濃度を抑制するに効果を奏する。

【００１８】本発明の第４の実施形態では、リン化硼素系半導体結晶層をリン化窒化硼素・インジウム（$B_{A}In_{D}N_{1-\delta}P_{\delta}$：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１、０＜δ≦１）混晶から構成し、リン化硼素系半導体結晶層上に設ける中間層を窒化アルミニウム・ガリウム・インジウム（$Al_{\gamma}Ga_{\beta}In_{\alpha}N$：０＜α≦０．５、０≦β＜１、０≦γ＜１、α＋β＋γ＝１）混晶から構成し、且つ活性層を窒化アルミニウム・ガリウム・インジウム（$A_{1Q}Ga_{R}In_{\gamma}N$：０＜Ｙ≦１、０≦Ｑ＜１、０≦Ｒ＜１、Ｑ＋Ｒ＋Ｙ＝１）混晶から構成する。ここでα≦０．５×Ｙとする。リン化窒化硼素・インジウム混晶からは、基板とする珪素単結晶に格子整合するリン化硼素系半導体結晶層を構成できる利点がある（特開２０００－２２２１１号公報参照）。また、窒化アルミニウム・ガリウム・インジウム混晶は、一種のワイドバンドギャップ（ｗｉｄｅ　ｂａｎｄｇａｐ）材料であるため、例えば、近紫外帯光或いは短波長可視帯光を出射するに好都合な活性層を構成できる。また、規定されたインジウム組成（α、但し０＜α≦０．５でα≦０．５×Ｙ）を有し、且つ活性層の構成元素を含んでなる窒化アルミニウム・ガリウム・インジウム（$Al_{\gamma}Ga_{\beta}In_{\alpha}N$：０＜α≦０．５、０≦β＜１、０≦γ＜１、α＋β＋γ＝１）混晶から構成した中間層は、活性

層の成長に於ける「成長核」を提供して、活性層の成膜を促進すると共に、インジウム組成（＝Ｙ）の均一な活性層をもたらせる。

【００１９】さらに本発明の第５の実施形態では、リン化硼素系半導体結晶層をリン化硼素・インジウム（B_AInDP：０＜Ａ≦１、０≦Ｄ＜１、Ａ＋Ｄ＝１）混晶から構成し、リン化硼素系半導体結晶層上に設ける中間層を窒化ガリウム・インジウム（$GaβInαN$：０＜$α$≦０．５、０≦$β$＜１、$α+β$＝１）混晶から構成し、活性層を窒化ガリウム・インジウム（$GaRInγN$：０＜Ｙ≦１、０≦Ｒ＜１、Ｒ＋Ｙ＝１）混晶から構成する。ここで$α$≦０．５×Ｙとする。B_AInDP混晶は構成元素がより少なく、従って、リン化硼素系半導体結晶層の形成を簡便とできる。特に、室温での禁止帯幅を約３ｅＶ前後とする単量体のリン化硼素（ＢＰ）結晶層からは、活性層（発光層）に対する障壁層（クラッド層）となるリン化硼素系半導体結晶層を構成できる。また、酸素（Ｏ）等の不純物を含む高抵抗のリン化硼素（ＢＰ）結晶層からは、例えば、ＦＥＴ用途の緩衝層を構成できる。また、中間層をインジウム組成は異にするものの、活性層と同様の材料から構成すれば、相互の格子ミスマッチ度を小と出来るため、ミスフィット（ｍｉｓｆｉｔ）転位等の結晶欠陥密度の低い良質の活性層を構成できる。特に、閃亜鉛鉱型の結晶体を混在したウルツ鉱型結晶からなる中間層は、結晶欠陥密度の少ない結晶性に優れる活性層をもたらすに貢献できる。

【００２０】ＩＩＩ－Ｖ族化合物半導体結晶からなる中間層は、リン化硼素系半導体結晶層或いは活性層と同様に、例えば、有機金属化学的気相堆積法（ＭＯＣＶＤ法）等の成長手段により成膜できる。例えば、トリエチル硼素（$(C_2H_5)_3B$）／シクロペンタジエニルインジウム（C_5H_5In）／ホスフィン（PH_3）原料系ＭＯＣＶＤ法に依り成膜できる。ルイス（Ｌｅｗｉｓ）塩基性のPH_3に対し、強度のルイス酸性を呈しないC_5H_5Inをインジウム原料とすれば、PH_3とのポリマー（ｐｏｌｙｍｅｒ）化反応が抑制され、常圧（略大気圧）下のＭＯＣＶＤ法でも良質のインジウムを含有する中間層を形成できる（日本国特許２０９８３８８号参照）。ＭＯＣＶＤ法に依り中間層を成膜するに際し、その層厚は、珪素単結晶基板上への硼素（Ｂ）及びインジウム（Ｉｎ）等のＩＩＩ族構成元素の原料の供給量及びその供給時間により制御できる。中間層のインジウム組成（＝$α$）は、ＩＩＩ族構成元素の供給量の総量に対するインジウム原料の供給量の濃度比率を変化させて調整する。また、中間層のキャリア濃度は、ＩＩＩ族構成元素の原料の供給量に対するＶ族構成元素の供給量の比率（所謂、Ｖ／ＩＩＩ比率）を適宜、選択することに依り、または不純物を故意に添加（ドーピング）して調整する。ｎ形の中間層を得るに適する不純物としては、珪素（Ｓｉ）、錫（Ｓｎ）、硫黄（Ｓ）、セレン（Ｓｅ）やテルル（Ｔｅ）等を例示できる。ｐ形のドーパント（ｄｏｐａｎｔ）には、亜鉛（Ｚｎ）、マグネシウム（Ｍｇ）、炭素（Ｃ）等がある。

【００２１】ＭＯＣＶＤ法により、珪素単結晶基板上に設けられた例えば、単量体のリン化硼素（ＢＰ）結晶からなるリン化硼素系半導体結晶層上に、窒化アルミニウム・ガリウム・インジウム（$AIγGaβInαN$：０＜$α$≦０．５、０≦$β$＜１、０≦$γ$＜１、$α+β+γ$＝１）混晶から構成される中間層を成膜するに際し、リン化硼素結晶層は約７５０℃～約１２００℃の範囲で、成膜するのが好ましい。約１２００℃を越える高温では、B_6P、$B_{13}P_2$等の多量体のリン化硼素結晶が生成され、単量体のリン化硼素からなる均質な結晶層が得られず不適である。中間層はそれより低温の約７００℃～約９５０℃の範囲で成膜するのが適する。インジウム組成（$α$）を大とする中間層程、成膜温度を低温とすると、平坦な表面の中間層が得られる。アルミニウム（ＡＩ）を含むＩＩＩ族窒化物半導体結晶層からなる中間層を成膜するには、成膜温度を、上記の温度範囲内で比較的高温とするのが適する。中間層上に積層する活性層を、インジウム組成は相違するものの、同様の結晶材料から構成すると、活性層を中間層と略同等の温度で簡便に形成できる利点がある。中間層或いは活性層のインジウム組成（$α$またはＹ）は、例えば、Ｘ線回折法、２次イオン質量分析法（ＳＩＭＳ）、オージェ（Ａｕｇｅｒ）分光分析法（ＡＥＳ）等の組成分析手段を利用して定量できる。

【００２２】

【作用】珪素単結晶基板とインジウムを含有するＩＩＩ族窒化物半導体結晶層からなる活性層との中間に設けられた、活性層のインジウム組成を基に規定されたインジウム組成を有する中間層は、活性層のインジウム組成を均一化させる作用を有する。また、表面の平坦性に優れる活性層をもたらす作用を有する。

【００２３】また、活性層のインジウム組成を基に規定されたインジウム組成を有し、且つ結晶型を相違する結晶体を含む多結晶層からなる中間層は、結晶性に優れる活性層をもたらす作用を有する。

【００２４】

【実施例】リン化硼素系半導体素子からなる発光ダイオード（ＬＥＤ）を作製した例に挙げて、本発明の内容を具体的に説明する。本実施例に係わるＬＥＤ１Ｂの平面模式図を図３に示す。また、図３に示す破線Ｘ－Ｘ’に沿ったＬＥＤ１Ｂの断面模式図を図４に示す。

【００２５】ＬＥＤ１Ｂ用途の積層構造体１Ａは、（１１１）結晶面を表面とする硼素（Ｂ）を添加したｐ形のＳｉ単結晶を基板１０１として構成した。基板１０１上には、トリエチル硼素（$(C_2H_5)_3B$）／ホスフィン（PH_3）／水素（H_2）系常圧ＭＯＣＶＤ法により、３５０℃で、ａｓ－ｇｒｏｗｎ状態で非晶質を主体とする

リン化硼素からなる緩衝層１０２を堆積した。緩衝層１０２の層厚は約１０ｎｍとした。緩衝層１０２の表面には、上記のＭＯＣＶＤ気相成長手段を利用して、１０５０℃で成長させたｐ形の単量体リン化硼素（ＢＰ）結晶からなるリン化硼素系半導体結晶層１０３を積層した。ｐ形のリン化硼素系半導体結晶層１０３のキャリア濃度は約$7\times10^{18}cm^{-3}$とし、また、層厚は約４００ｎｍとした。ｐ形のリン化硼素系半導体結晶層１０３をなす単量体のＢＰ層の室温での禁止帯幅は大凡、３．０ｅＶであった。

【００２６】ｐ形のリン化硼素系半導体結晶層１０３上には、トリメチルガリウム（$(CH_3)_3Ga$）／シクロペンタジエニルインジウム（C_5H_5In）／アンモニア（NH_3）／H_2系常圧ＭＯＣＶＤ法により、インジウム組成を０．０６（＝６%）とするウルツ鉱結晶型のｎ形窒化ガリウム・インジウム（$Ga_{0.94}In_{0.06}N$）からなる中間層１０４を積層した。中間層１０４の成膜温度は８００℃とし、また、層厚は１５ｎｍとした。透過型電子顕微鏡（ＴＥＭ）を用いた断面ＴＥＭ像及び制限視野電子線回折図形から、中間層１０４の内部には閃亜鉛鉱型の結晶体１０４ａの存在が確認された。結晶体１０４ａは特に、リン化硼素系半導体結晶層１０３との接合界面の近傍の領域に多く存在していた。結晶体１０４ａの大きさは概ね、約２ｎｍから約５ｎｍであった。

【００２７】中間層１０４の表面上には、インジウム組成を０．１５（＝１５%）とするウツツ鉱型の珪素（Ｓｉ）ドープｎ形窒化ガリウム・インジウム（$Ga_{0.85}In_{0.15}N$）からなる活性層（発光層）１０５を堆積した。活性層１０５の成膜温度は、中間層１０４と同じく８００℃とし、層厚は約３００ｎｍとした。また、活性層１０５のキャリア濃度は約$6\times10^{17}cm^{-3}$に設定した。２次イオン質量分析法（ＳＩＭＳ）に依り計測した活性層１０５内部のインジウム組成の深さ方向の分布は図５に示す如く、中間層１０４との接合界面に至る迄、約０．１５と均一であった。中間層１０４との接合界面の近傍の活性層１０５の内部領域に於けるリン（Ｐ）原子の濃度は約$1\times10^{18}cm^{-3}$未満であり、ｐ形のリン化硼素系半導体結晶層１０３より拡散して来るリン（Ｐ）原子に対する中間層１０４の捕獲作用が顕現されていた。また、断面ＴＥＭ技法による観察では、リン化硼素系半導体層１０３から活性層１０５内に貫通してくる転位は殆ど視認されなかった。

【００２８】活性層１０５上には、単量体のリン化硼素（ＢＰ）からなるｎ形のリン化硼素系半導体結晶層１０６を積層した。ｎ形のリン化硼素系半導体結晶層１０６のキャリア濃度は約$1\times10^{19}cm^{-3}$とし、また、層厚は約４００ｎｍとした。ｎ型のリン化硼素系半導体結晶層１０６は、室温での禁止帯幅を大凡、３．０ｅＶとする単量体のリン化硼素結晶より構成した。ｎ形のリン化硼素系半導体結晶層１０６及びｐ形のリン化硼素系半導体結晶層１０３と活性層１０５とから、中間層１０４とｐ形リン化硼素系半導体結晶層１０３とのｐｎ接合構造を備えたダブルヘテロ（ＤＨ）構造の発光部を構成した。

【００２９】ｎ形のリン化硼素系半導体結晶層１０６の表面の中央部には、結線用の台座電極を兼ねる３層構造の表面オーミック電極１０７を配置した。表面オーミック電極１０７は直径を約１２０μｍとする円形とした。表面オーミック電極１０７の、ｎ形リン化硼素半導体結晶層１０６と接触する部位１０７ａは、金（Ａｕ）・ゲルマニウム（Ｇｅ）合金の真空蒸着膜（膜厚≒７００ｎｍ）から構成した。Ａｕ・Ｇｅ真空蒸着膜１０７ａの上には、ニッケル（Ｎｉ）真空蒸着膜（膜厚≒１００ｎｍ）１０７ｂ被着させた。Ｎｉ真空蒸着膜１０７ｂの上には、Ａｕ真空蒸着膜（膜厚≒１０００ｎｍ）１０７ｃを被着させた。一方、ｐ形Ｓｉ単結晶基板１０１の導電性を活用して、基板１０１の裏面の略全面には、アルミニウム（Ａｌ）真空蒸着膜（膜厚≒７００ｎｍ）からなる裏面オーミック電極１０８を配置した。その後、積層構造体１Ａを、基板１０１のＳｉ単結晶の＜２１１＞結晶方向に平行及び垂直な方向に沿って裁断して、一辺を約３５０μｍとする正方形のＬＥＤ１Ｂとした。

【００３０】表面オーミック電極１０７と裏面オーミック電極１０８との間に、順方向に２０ミリアンペア（ｍＡ）の動作電流を通流し、ＬＥＤ１Ｂの発光特性を調査した。発光中心波長は４６０ｎｍとなった。中間層１０４のインジウム組成（＝０．０６）を、活性層１０５のインジウム組成（＝０．１５）の半値（＝１／２）以下としたため、この主たる発光スペクトル以外に副次的な発光は認められず、発光は半値幅（＝ＦＷＨＭ）を約２０ｎｍとする単色性に優れるものであった。また、結晶型の相違する結晶体を含む構成からなる中間層１０４の作用により、貫通転位の少ない活性層１０５をもたらすことが出来たため、一般の積分球を使用してチップ（ｃｈｉｐ）状態で計測される輝度は９ミリカンデラ（ｍｃｄ）となった。また、通常の電流ー電圧（Ｉ－Ｖ）特性から求められた順方向電圧（Ｖｆ）は約３．７Ｖ（順方向電流＝２０ｍＡ）であった。また、逆方向電流が１０μＡに到達する際の電圧である逆方向電圧（Ｖｒ）は約１０Ｖ以上であり、良好なｐｎ接合特性（整流特性）が顕現された。以上、本発明に依って、高い発光強度を呈しつつ且つ耐圧性に優れるリン化硼素系半導体ＬＥＤが提供される結果となった。

【００３１】

【発明の効果】珪素単結晶からなる基板と、基板上に設けられたリン化硼素系半導体結晶層と、リン化硼素系半導体結晶層上に設けられた活性層の下地層となる中間層と、中間層上にインジウム組成をＹ（０＜Ｙ≦１）とするＩＩＩ族窒化物半導体結晶からなる活性層とを利用してリン化硼素系半導体素子を構成するに際し、本発明で

は、活性層をなすＩＩＩ族窒化物半導体結晶層のインジウム組成の１／２以下のインジウム組成のＩＩＩ－Ｖ族化合物半導体から中間層を構成することとしたので、例えば、ＬＥＤ等のリン化硼素系半導体発光素子にあって、発光の単色性を乱す副次的な発光を回避でき、単色性に優れる発光素子をもたらすに効果を奏する。

【００３２】また本発明では、中間層のインジウム組成を、活性層をなすＩＩＩ族窒化物半導体結晶層のインジウム組成の１／２以下とするに加え、結晶型の相違する結晶体を含む多結晶層から中間層を構成することとしたので、例えば、発光強度と電気的な耐圧特性に優れるリン化硼素系半導体素子からなる発光ダイオードを提供できた。

【図面の簡単な説明】

【図１】中間層のインジウム組成が高い場合の活性層の深さ方向のインジウム組成の分布を示す図である。

【図２】中間層がインジウムを含まない場合の活性層の深さ方向のインジウム組成の分布を示す図である。

【図３】本発明の実施例に係るＬＥＤの平面模式図である。

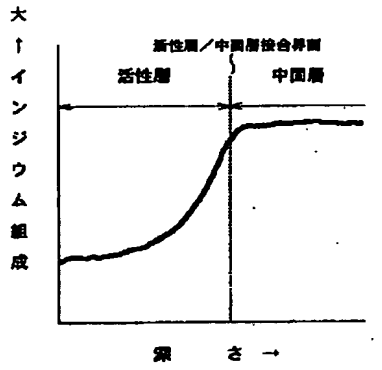
【図４】図３に示す破線Ｘ－Ｘ’に沿ったＬＥＤの断面模式図である。

【図５】本発明の実施例に係わる活性層の深さ方向のインジウム組成の分布を示す図である。

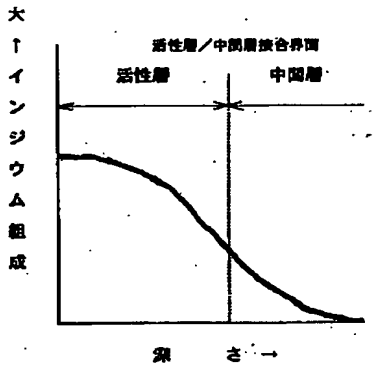
【符号の説明】

１Ａ　発光素子（ＬＥＤ）用途積層構造体
１Ｂ　ＬＥＤ
１０１　基板
１０２　緩衝層
１０３　ｐ形のリン化硼素系半導体結晶層
１０４　中間層
１０４ａ　結晶体
１０５　活性層
１０６　ｎ形のリン化硼素系半導体結晶層
１０７　表面オーミック電極
１０７ａ　Ａｕ・Ｇｅ真空蒸着膜
１０７ｂ　Ｎｉ真空蒸着膜
１０７ｃ　Ａｕ真空蒸着膜
１０８　裏面オーミック電極

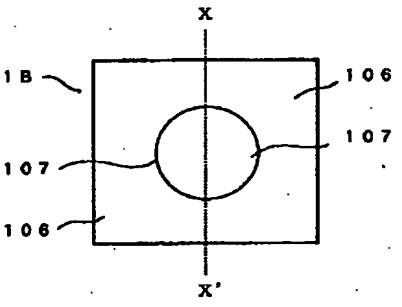
【図１】



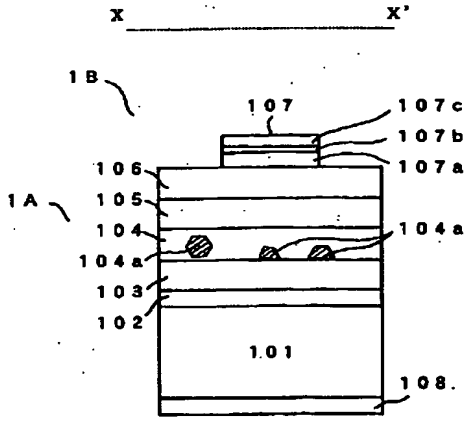
【図２】



【図３】



【図４】



【図５】